

# Everything you ever wanted to know about debug interfaces

Talk @ Fri3d Camp 2022

**PorocYon**

Slides: <https://pcy.be/fc22>

# TOC

Introduction

Arduino and AVR

ESP32

ARM Cortex-M

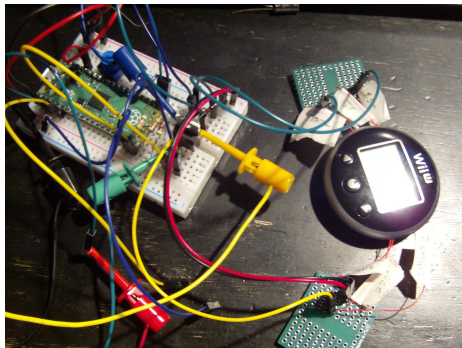
TI MSP430

Renesas RL78

# Whoami

- ▶ Demoscener and hardware hacker
- ▶ Dumped DSi ARM7 boot ROM and Wii Fit U Meter flash using glitching
- ▶ Linux demoscene 4k intro tooling, ...

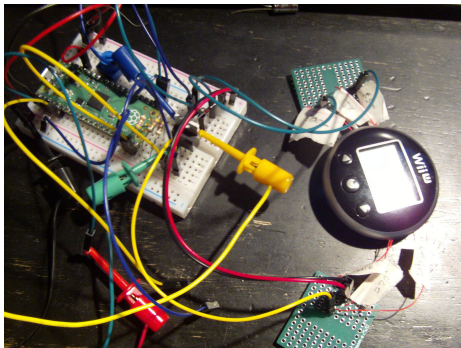
# Wii Fit U Meter



- ▶ Similar to Pokéwalker, but different MCU
- ▶ No IR exploit known ( $\leftrightarrow$  Pokéwalker)
- ▶ VFI attack inspired by fail0verflow on the PS4 Syscon<sup>2</sup>

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# Wii Fit U Meter



- ▶ Similar to Pokéwalker, but different MCU
- ▶ No IR exploit known ( $\leftrightarrow$  Pokéwalker)
- ▶ VFI attack inspired by fail0verflow on the PS4 Syscon<sup>2</sup>
- ▶ Targetting the debug interface!

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# Debug interfaces

- ▶ Can teach you how a microcontroller *actually* works
- ▶ Often poorly documented, sadly

1	(N/A)	Always write 0, same as previous families.
2	(N/A)	Always write 0, same as previous families.
3	WAIT	Wait signal to the CPU. Read only. 1 = CPU clock stopped - waiting for an operation to 0 = CPU clock not stopped
4	BYTE	Controls the BYTE signal of the CPU used for mem 1 = Byte (8-bit) access 0 = Word (16-bit) access
12	RELEASE_LBYTE0	Release control bits in low byte from JTAG control. 00 = All bits are controlled by JTAG if TCE1 is 1
13	RELEASE_LBYTE1	01 = RW (bit 0) and BYTE (bit 4) are released from 10 = RW (bit 0) HALT (bit 1), INTREQ (bit 2), and E 11 = Reserved
14	INSTR_SEQ_NO0	Instruction sequence number. Read only.

# Debug interfaces

- ▶ Creating a CPU: “black magic”
- ▶ Creating a debugger: “extreme ultra evil elite black magic”



# I assume you:

- ▶ know what a debugger is (or have used one)
- ▶ have an idea about what an assembly instruction is
- ▶ have a vague idea what Arduino is
- ▶ have a very vague concept of digital hardware (eg. have played Turing Complete)

# What does this button do?



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File Edit Sketch Tools Help
[Upload] [New] [Open] [Save] [Find]
avr7g
1 void setup() {
2   // put your setup code here, to run once:
3   pinMode(2, OUTPUT);
4   Serial.begin(9600); while (!Serial) ;
5 }
6
7 #define NUM_GLITCH_LOOPS 0xffff
8
9 void loop() {
10  static char buf[64];
11  static volatile uint16_t buf2[64];
12  volatile uint16_t a, b = NUM_GLITCH_LOOPS;
13  volatile uint8_t c;
14
15  for (c = 0; c < 4; ++c) {
16    b = NUM_GLITCH_LOOPS;
17    for (a = 0; a < NUM_GLITCH_LOOPS; ++a)
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```

# avrdude

```
Global variables use 404 bytes (19%) of dynamic memory, leaving 1644 bytes for local variables. Maximum is 2048 bytes.
/usr/bin/avrdude -C/etc/avrdude.conf -v -patmega328p -carduino -P/dev/ttyACM0 -b115200 -D -Uflash:w:/tmp/arduino_build_178202/avrtgt.ino.hex:i

avrdude: Version 7.0
Copyright (c) Brian Dean, http://www.bdmicro.com/
Copyright (c) Jelte Wijkstra
```

```
Programmer Type : Arduino
Description      : Arduino
Hardware Version: 3
Firmware Version: 4.4

avrdude: AVR device initialized and ready to accept instructions.

Reading | #####

avrdude: Device signature = 0x1e950f (probably atmega328p)
avrdude: reading input file "/tmp/arduino_build_178202/avrtgt.ino.hex"
avrdude: writing flash (3304 bytes):

Writing | #####
```

# avrdude

```
Global variables use 404 bytes (19%) of dynamic memory, leaving 1644 bytes for local variables. Maximum is 2048 bytes.
/usr/bin/avrdude -C/etc/avrdude.conf -v -patmega328p -carduino -P/dev/ttyACM0 -b115200 -D -Uflash:w:/tmp/arduino_build_178202/avrtgt.ino.hex:i

avrdude: Version 7.0
Copyright (c) Brian Dean, http://www.bdmicro.com/
Copyright (c) Joerg Wunsch
```

- ▶ avrdude: does heavy lifting of the actual upload
- ▶ From the avrdude documentation:  
*The Arduino [...] is supported via its own programmer type specification “arduino”. This programmer works for the Arduino Uno Rev3 or any AVR that runs the Optiboot bootloader.*

# avrdude

```
Global variables use 404 bytes (19%) of dynamic memory, leaving 1644 bytes for local variables. Maximum is 2048 bytes.
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avrdude: Version 7.0
Copyright (c) Brian Dean, http://www.bdmicro.com/
Copyright (c) Joerg Wunsch
```

- ▶ avrdude: does heavy lifting of the actual upload
- ▶ From the avrdude documentation:  
*The Arduino [...] is supported via its own programmer type specification "arduino". This programmer works for the Arduino Uno Rev3 or any AVR that runs the Optiboot bootloader.*
- ▶ Optiboot??

# Optiboot

- ▶ 'Bootloader': small program in flash that loads your Arduino sketch
- ▶ But the ATmega328P cannot speak USB directly

# Optiboot

- ▶ 'Bootloader': small program in flash that loads your Arduino sketch
- ▶ But the ATmega328P cannot speak USB directly
- ▶ ⇒ Secret second ATmega on the Arduino!

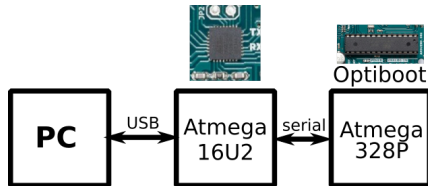
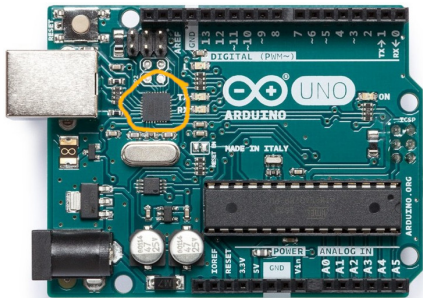


image source: <https://corzotech.com/en/boards/202-arduino-uno-rev3-with-long-pins-8058333491769.html>  
<https://github.com/arduino/ArduinoCore-avr/tree/master/bootloaders/optiboot>

<https://github.com/arduino/ArduinoCore-avr/tree/master/firmwares/atmegaxxu2>

Is this an answer

**No!**

How does the bootloader get inside the ATmega328P?

How does the USB↔serial firmware get inside the ATmega16U2?

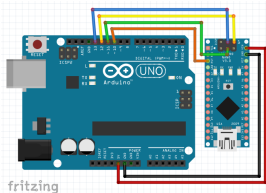


# ICSP

## In Circuit Serial Programming

- ▶ SPI-based protocol
- ▶ Device identification
- ▶ Read & write memory
- ▶ No debug capability

## Arduino-ISP!



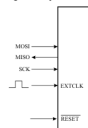
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image sources: ATmega328P datasheet 42735,  
<https://arduinoaddiction.blogspot.com/2016/02/program-arduino-nano-via-uno-with-icsp.html>,  
<https://www.e-tinkers.com/2020/03/do-you-know-arduino-spi-and-arduino-spi-library/>

### 31.8. Serial Downloading

Both the Flash and EEPROM memory arrays can be programmed. The serial interface consists of pins MISO, MOSI, SCK, and RESET. When the RESET pin is pulled to GND, the Programming Enable instruction operations can be executed.

Figure 31-6. Serial Programming and Verify

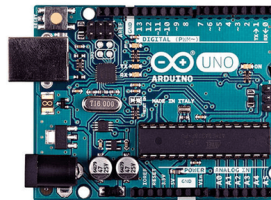


### 31.8.3. Serial Programming Instruction Set

This section describes the Instruction Set

Table 31-17. Serial Programming Instruction Set

Instruction/Operation
Programming Enable
Chip Erase (Program Memory/EEPROM)
Poll RDY/BSY
Load Instructions



#### ICSP Header

In-Circuit Serial Programming Header for SPI Communication

MISO	VCC
SCK	MOSI
RST	GND

# Debug?

## debugWire

- ▶ Single-wire UART
- ▶ Simple command set:  
command X = do XYZ
- ▶ Access to CPU registers & breakpoints
- ▶ No official docs, but  
reverse-engineered

<http://www.ruemohr.org/docs/debugwire.html>

## Resuming execution

```
D0 00 00 xx -- set PC, xx = 40/60 - 41/61 - 5
D1 00 01 -- set breakpoint (single step in tr
D0 00 00 30 -- set PC and G0
```

## Resuming from a SW BP

```
D0 00 00 79/59 -- set PC
D1 00 01 -- set breakpoint (single step in tr
D2 ii ii -- load the instruction replaced by
D0 00 00 32 -- set PC and G0
```

## Step Out -- D1 isn't used

```
D0 00 00 63/43 -- set PC
D0 00 00 30 -- set PC and G0
```

source: see URL

## Annoying limitation

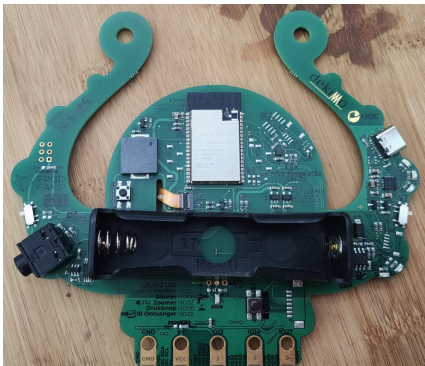
- ▶ dW ↔ ICSP: can only use one
- ▶ Annoying mode switches between the two
  
- ▶ New protocols: **T**iny **P**rogramming Interface +  
(**U**nified) **P**rogram and **D**ebug Interface
- ▶ Used in new AVR<sup>s</sup> (tinyAVR, megaAVR, AVR-Dx)



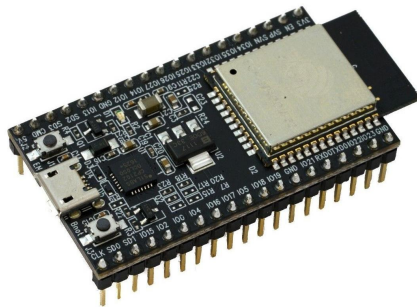
source: Hackaday



# Next target



source: <https://github.com/Fri3dCamp/badge-2020>



source: <https://www.nabto.com/guide-to-iot-esp-32/>

# ESP32 programming

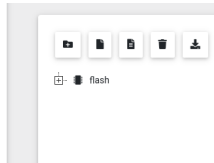
```
Connecting...
Chip is ESP32-S2
Features: WiFi, No Embedded Flash, No Embedded PSRAM,
Crystal is 40MHz
MAC: 60:55:f9:e0:8c:a2
Uploading stub...
Running stub...
Stub running...
Changing baud rate to 460800
Changed.
Configuring flash size...
Auto-detected Flash size: 4MB
Flash will be erased from 0x00001000 to 0x00006fff...
Flash will be erased from 0x00010000 to 0x00039fff...
Flash will be erased from 0x00008000 to 0x00008fff...
Flash params set to 0x022f
Compressed 21312 bytes to 13422...
Writing at 0x00001000... (100 %)
Wrote 21312 bytes (13422 compressed) at 0x00001000 in
Hash of data verified.
Compressed 168544 bytes to 100640...
Writing at 0x00010000... (14 %)
Writing at 0x0001af26... (28 %)
```



Apps

Programming &amp; Files

Settings



## Fri3d Flasher



Download hieronder een firmwarebestand en klik dan hier om het te uploaden.

Begin the flashen

# A bootrom!

## First stage bootloader

After SoC reset, PRO CPU will start running immediately, executing reset vector code, while APP CPU will be held in reset. During startup process, PRO CPU does all the initialization. APP CPU reset is de-asserted in the `call_start_cpu0` function of application startup code. Reset vector code is located in the mask ROM of the ESP32 chip and cannot be modified.

2. For power-on reset, software SOC reset, and watchdog SOC reset: check the `GPIO_STRAP_REG` register if a custom boot mode (such as UART Download Mode) is requested. If this is the case, this custom loader mode is executed from ROM. Otherwise, proceed with boot as if it was due to software CPU reset. Consult ESP32 datasheet for a description of SoC boot modes and how to execute them.

source: <https://docs.espressif.com/projects/esp-idf/en/latest/esp32/api-guides/startup.html>

- ▶ Bootrom: immutable program running in CPU
- ▶ Uses UART to load program & save to flash
- ▶ ↔ bootloader: this not in flash!

# A bootrom!

## First stage bootloader

After SoC reset, PRO CPU will start running immediately, executing reset vector code, while APP CPU will be held in reset. During startup process, PRO CPU does all the initialization. APP CPU reset is de-asserted in the `call_start_cpu0` function of application startup code. Reset vector code is located in the mask ROM of the ESP32 chip and cannot be modified.

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- ▶ Bootrom: immutable program running in CPU
- ▶ Uses UART to load program & save to flash
- ▶ ↔ bootloader: this not in flash!
- ▶ .. can't do debug, but ESP32 has a debugger!











## JTAG on the ESP32

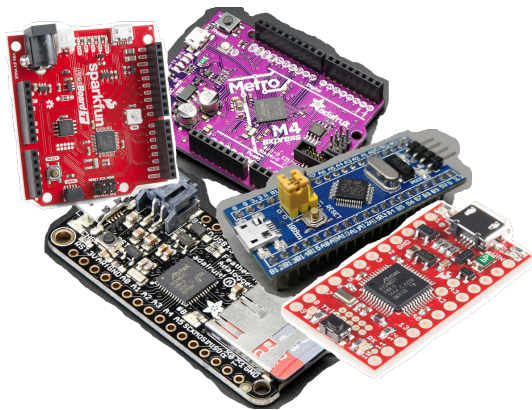
```
#define TAPINS_PWRCTL      0x08 84 /*OCD registers */
#define TAPINS_PWRSTAT    0x09 85 #define NARADR_OCDID      0x40
#define TAPINS_NARSEL     0x1C 86 #define NARADR_DCRCLR   0x42
#define TAPINS_IDCODE     0x1E 87 #define NARADR_DCRSET   0x43
#define TAPINS_BYPASS     0x1F 88 #define NARADR_DSR      0x44
                                89 #define NARADR_DDR      0x45
#define TAPINS_PWRCTL_LEN 8     90 #define NARADR_DDREXEC  0x46
#define TAPINS_PWRSTAT_LEN 8    91 #define NARADR_DIRBEXEC 0x47
#define TAPINS_NARSEL_ADRLLEN 8 92 #define NARADR_DIR0    0x48
#define TAPINS_NARSEL_DATALEN 32 93 #define NARADR_DIR1    0x49
#define TAPINS_IDCODE_LEN 32    94 /*... */
#define TAPINS_BYPASS_LEN 1     95 #define NARADR_DIR7    0x4F

for (unsigned int i = 0; i < xtensa->core_config->user_regs_num; i++) {
  > if (!xtensa_reg_is_readable(xtensa->core_config->user_regs[i].flags,
  > continue;
  > xtensa_queue_exec_ins(xtensa, XT_INS_RUR(xtensa->core_config->user_regs[i].addr));
  > xtensa_queue_exec_ins(xtensa, XT_INS_WSR(XT_SR_DDR, XT_REG_A3));
  > xtensa_queue_dbg_reg_read(xtensa, NARADR_DDR, regvals[i]);
  > if (debug_dsrs)
  > xtensa_queue_dbg_reg_read(xtensa, NARADR_DSR, dsrs[i]);
}
```

- ▶ No docs, but OpenOCD source code
- ▶ Xtensa 'NAR', 'TRAX', and CoreSight CTI
- ▶ 'NAR': send single instructions to CPU, use DDR as data channel

<https://github.com/espressif/openocd-esp32>

# Ever seen these?



ATSAMD, STM32, LPCxx, K32L, RP2040, ...

sources: Adafruit and Sparkfun product catalogs, <https://stm32-base.org/boards/STM32F103C8T6-Blue-Pill.html>

# Bootroms



## AN2606 Application note

STM32™ microcontroller  
system memory boot mode

### Introduction

The bootloader is stored in the internal boot ROM memory (system memory) of STM32 devices. It is programmed by ST during production. Its main task is to download the application program to the internal Flash memory through one of the available serial peripherals (USART, CAN, USB, etc.). A communication protocol is defined for each serial interface, with a compatible command set and sequences.

The main features of the bootloader are the following:

- It uses an embedded serial interface to download the code with a predefined communication protocol
- It transfers and updates the Flash memory code, the data, and the vector table sections

- ▶ Many of these have a UART bootrom
- ▶ Similar features: read & write flash, access lock, ...
- ▶ *Bootrom controls debug enable/disable* ⇒ glitch target

# ARM ADI

## Arm® Debug Interface Architecture Specification ADIV5.0 to ADIV5.2

- ▶ ARM debug is standardized and documented!
- ▶ Many layers: SWD - DP - MEM-AP



# SWD and the Debug Port

- ▶ Half-duplex synchronous serial
- ▶ Few registers that give access to *access port*
- ▶ Simple! ( $\leftrightarrow$  JTAG)
- ▶ Access to MCU memory
- ▶ Extra secret registers for device info & debug control

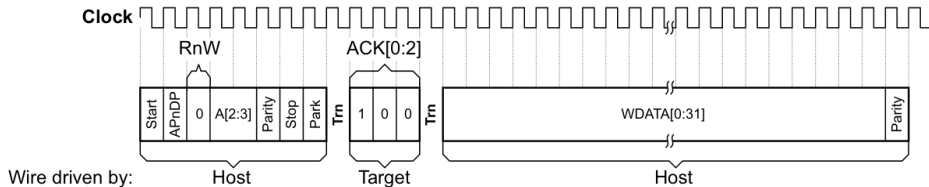


image source: ARM Debug Interface Architecture Specification v5

## SWD and the Debug Port

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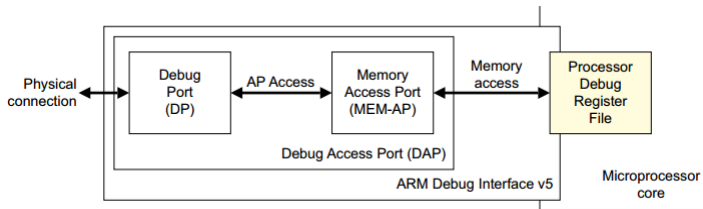


image source: ARM Debug Interface Architecture Specification v5

# MEM-AP

Debug resource	Address Range
Data Watchpoint and Trace	0xE0001000-0xE0001FFF
Breakpoint unit	0xE0002000-0xE0002FFF
SCS	0xE000ED00-0xE000EEFF
System Control Block	0xE000ED00-0xE000ED8F
Debug Control Block	0xE000EDF0-0xE000EEFF
ARMv6-M ROM table	0xE00FF000-0xE00FFFFF

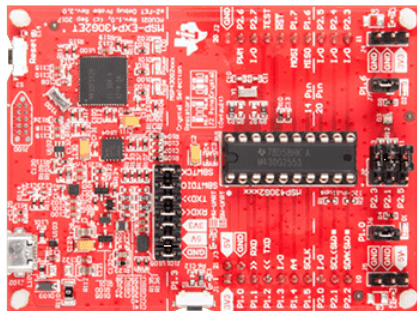
source: ARMv6-M Architecture Reference Manual

- ▶ Accessed through SWD-DP
- ▶ Access to MCU memory
- ▶ ROM tables
- ▶ Extra registers for debug

# PDP-11 in a microcontroller

```
 Energia_Rocks.ino | Energia 1.6.10E18
 Energia_Rocks.ino
1 #define LED_RED_LED
2
3 // the setup routine runs once when you press reset:
4 void setup() {
5   // initialize the digital pin as an output.
6   pinMode(LED, OUTPUT);
7 }
8
9 // the loop routine runs over and over again forever:
10 void loop() {
11   digitalWrite(LED, HIGH); // turn the LED on (HIGH is the voltage level)
12   delay(1000); // wait for a second
13   digitalWrite(LED, LOW); // turn the LED off by making the voltage LOW
14   delay(1000); // wait for a second
15 }
Done Saving.
15 RED LaunchPad w/ msp432 EMT (48MHz) on /dev/tty.usbmodemM4321001
```

source: <https://energia.nu/>



source: <https://www.ti.com/tool/MSP-EXP430G2ET>

# Another bootrom

*User's Guide*

## **MSP430™ Flash Devices Bootloader (BSL)**



### ABSTRACT

The MSP430™ bootloader (BSL) (formerly known as the bootstrap loader) allows users to communicate with embedded memory in the MSP430 microcontroller (MCU) during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

To use the bootloader, a specific BSL entry sequence must be applied. An added sequence of commands initiates the desired function. A bootloading session can be exited by continuing operation at a defined user program address or by the reset condition.

If the device is secured by disabling JTAG, it is still possible to use the BSL. Access to the MSP430 MCU memory through the BSL is protected against misuse by the BSL password. The BSL password is equal to the content of the interrupt vector table on the device.

source: <https://www.ti.com/lit/pdf/slau319>

- ▶ UART/I<sup>2</sup>C
- ▶ Read from flash is password-protected
- ▶ Erase flash on wrong password!

# Another bootrom

User's Guide

## MSP430™ Flash Devices Bootloader (BSL)



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The MSP430™ bootloader (BSL) (formerly known as the bootstrap loader) allows users to communicate with embedded memory in the MSP430 microcontroller (MCU) during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

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source: <https://www.ti.com/lit/pdf/slau319>

- ▶ UART/I<sup>2</sup>C
- ▶ Read from flash is password-protected
- ▶ Erase flash on wrong password!
- ▶ “authenticated” flag stored in RAM...
- ▶ Target ‘authenticated’ check for RAM write command

# Debugger woes

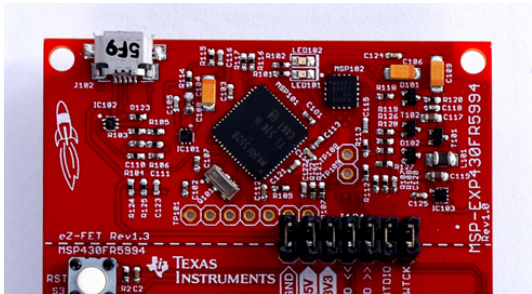
User's Guide

## MSP430™ Programming With the JTAG Interface



### ABSTRACT

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430™ flash-based and FRAM-based microcontroller families using the JTAG communication port.



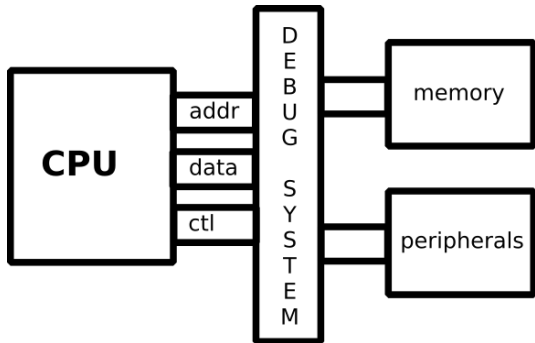
sources: <https://www.ti.com/lit/pdf/slau320>,

- ▶ Every devboard has a debugger
- ▶ Documented in a PDF
- ▶ ... kinda



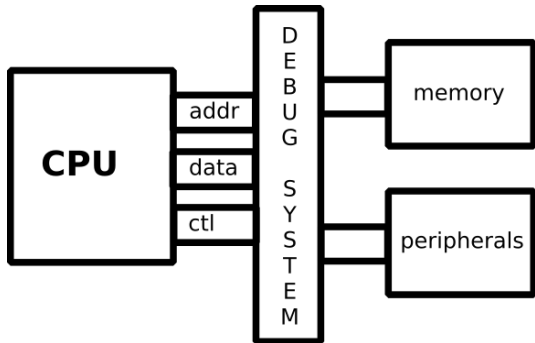


## Debug layer



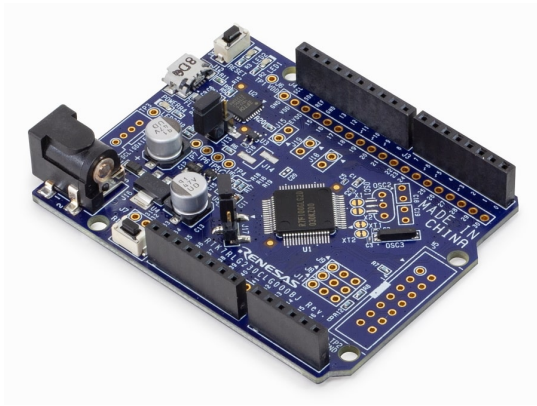
- ▶ CPU is connected to outside world and memory using the *system bus*
- ▶ Debug system: sit between CPU and bus
- ▶ Control addresses, data, and CPU signals

## Debug layer



- ▶ CPU is connected to outside world and memory using the *system bus*
- ▶ Debug system: sit between CPU and bus
- ▶ Control addresses, data, and CPU signals
- ▶ Very low-level control: detailed but hard to use

# Z80, but worse



source: <https://www.renesas.com/sites/default/files/rl78-g23-64p-fpb-board.jpg>

# Bootrom time



APPLICATION NOTE

RL78 Microcontrollers

RL78 Microcontrollers (RL78 Protocol A)

Programmer Edition

R01AN0815EJ0100  
Rev. 1.00  
Nov 7, 2011**Introduction**

This application note is intended for users who understand the functions of the RL78 microcontrollers and who will use this product to design application systems.

The purpose of this application note is to help users understand how to develop dedicated flash memory programmers for rewriting the internal flash memory of the RL78 microcontrollers.

source: <https://www.renesas.com/eu/en/document/apn/>

rl78-microcontrollers-rl78-protocol-programmer-edition-application-note-rev100

- ▶ UART bootrom
- ▶ Documented in PDF
- ▶ No flash read command ⇒ need something better





## Only the beginning

- ▶ Skipped eg. ARM CTI, MSP430 EEM, instruction tracing, EnergyTrace, ...
- ▶ More detail in protection mechanisms
- ▶ Other protocols
  - ▶ RISC-V
  - ▶ Nexus (OpenMSP430, AVR32, MPC/SPC, ...)
  - ▶ PIC
  - ▶ STM8 SWIM
  - ▶ MAXQ JTAG
  - ▶ EFM8 C2
  - ▶ ...
- ▶ History (eg. old ARM EmbeddedICE)
- ▶ Core↔core debug (Nailgun hack!<sup>1</sup>)
- ▶ How to actually implement this

<sup>1</sup>*Understanding the Security of ARM Debugging Features, Ning & Zhang* 

# Conclusion

- ▶ Debug systems are interesting
- ▶ Many different ways of making one
  
- ▶ Attractive target for hacking
- ▶ Need to understand how they work to know the risks
- ▶ But companies won't tell you enough to know the risks



## Questions

# Questions?

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Slides available at <https://pcy.be/fc22>